

		Alpha			HP		IBM			MIPS		Sun			
Parameter		21164	21264	21364	PA 8000	PA 8500	PowerPC 604	PowerPC 604e	PowerPC 620	Power3	R10000	R12000	UltraSparc I	UltraSparc II	UltraSparc III
Fetch	L1 I-Cache Size	KB	8	64	N/A	512	16	32	32	32	32	32	16	16	32
	L1 I-Cache Associativity	Ways	1	2	N/A	4	4	8	128?	2	2	2	2	2	4
	L1 I-Cache Block Size	Bytes	32	64	N/A	N/A	32	64	128	64	32	32	32	32	32
	L1 I-Cache Replacement Policy	N/A	N/A	X?	N/A	N/A	LRU	N/A	N/A	LRU	LRU	LRU	LRU	LRU?	pseudo-Random
	L1 I-Cache Latency	Cycles	2?	2?	N/A	2	1/2?	1	1	1	1/2?	1/2?	1?	2/3?	2
	Instruction Fetch Queue Entries	Entries	8?	N/A?	N/A?	N/A?	8?	8	12	4?	4?	4?	12	12	20
	BPred Type	N/A	Hint+BHT?	Hybrid McFarling	Hint+BHT?	X	Bimodal	4	4	8?	5	5	Hint+BHT?	Hint+BHT?	Gshare
	BPred Misprediction Penalty	Cycles	Average: 5	Average: 11+	6	"Large"	4?	3	3	3	3	3	4	4	8?
	Return Address Stack Entries	Entries	12	32	X?	X	8?	N/A	N/A	N/A	N/A	N/A	N/A?	4	8
	BTB Configuration	N/A	N/A?	N/A	32-Entry, FA	64-Entry, Full	256-Entry, 2-Way	256-Entry, 2-Way	256-Entry, 2-Way	N/A	32-Entry, 2-Way	N/A?	1024?	X?	X?
Execute	RUU Entries	Entries	N/A?	35?	56	56?	16	16	32?	32	48	N/A	N/A?	N/A?	
	Int ALUs	N/A	(2 GP + 2 Addr Calc)	4	4	4	2	2	2	2	2	2	2	2	
	Int ALU Latencies	Cycles	0/1/2	1/2	1	1	1	1	1	1	1	1	1	1	
	Int ALU Throughputs	Cycles	1?	1	1?	1?	1	1?	1?	1?	1	1	1	1?	
	FP ALUs	N/A	2	2	2	2	1	1	2	2	1	2	2	2?	
	FP ALU Latencies	Cycles	4	4	3	3	3	3	4	4	2	2	3	4	
	FP ALU Throughputs	Cycles	X?	1	1	1	1	1	1	1	1	1	1	1	
	Int Multi/Div	N/A	N/A	N/A	N/A	N/A	1	1	1	1	N/A	N/A	N/A	N/A	
	Int Multiply Latency	Cycles	32-bit: 8, 64-bit: 12,14	7	1	32-bit: 3-4, 64-bit: 3-9	16-bit: 3, 32-bit: 4	3	32-bit:3-4, 64-bit: 3-9	32-bit: 5/6, 64-bit: 9/10	5/35?	5-35	5-35	6-9	
	Int Divide Latency	Cycles	N/A?	N/A?	1/17?	32-bit: 21, 64-bit: 37	20	37	32-bit:21, 64-bit: 37	32-bit: 34/35, 64-bit: 66/67	67	64	40-70		
Int Multiply Throughput	Cycles	32-bit: 4, 64-bit: 8	1?	1	1	16-bit: 1, 32-bit: 2	1	1?	35	X?	5-35	1?			
Int Divide Throughput	Cycles	N/A?	N/A?	1/17?	19	37?	21,37?	67	X?	64	40-70				
FP Multi/Div	N/A	N/A	N/A	2	2	N/A	N/A	N/A	2	N/A	N/A	N/A			
FP Multiply Latency	Cycles	4?	4	3	3	3	32-bit: 3-4, 64-bit: 3-4	2	3	3	4				
FP Divide Latency	Cycles	Average: 19,31 (SP,DP)	12,15 (SP,DP)	17,31 (SP,DP)	17,31?	18,31 (SP,DP)	18	32-bit: 14-21, 64-bit: 18-25	32-bit: 12, 64-bit: 19	12,22 (SP/DP)	12,22 (SP,DP)	17,20 (SP/DP)			
FP Square Root Latency	Cycles	N/A	18,33 (SP,DP)	X,31 (SP,DP)?	17,31?	N/A	22	32-bit: 14-23, 64-bit: 22-31	32-bit: 18, 64-bit: 33	12,22 (SP/DP)?	12, 22 (SP,DP)	24,24 (SP,DP)			
FP Multiply Throughput	Cycles	X?	1	1	1	1	1	1	1	1	1	1			
FP Divide Throughput	Cycles	X?	9,12 (SP,DP)	17,31 (SP/DP)	17,31?	18,31 (SP,DP)	18	32-bit: 14, 64-bit: 21	12,22 (SP/DP)	12,22 (SP/DP)	17,20 (SP/DP)				
FP Square Root Throughput	Cycles	N/A	15,30 (SP,DP)	X,31 (SP,DP)?	17,31?	N/A	22	32-bit: 20, 64-bit: 35	12,22 (SP/DP)?	12, 22 (SP,DP)	24,24 (SP,DP)				
LSQ Entries	Entries	12?	64?	28?	28?	Load: 4, Store: 6?	Load: X, Store: 16?	16	Load: 9; Store: 8	Load: 9; Store: 8?	Load: X; Store: 8?				
Memory Ports	Ports	2	2	2	2?	2	2/4?	X	X?	X?	X?				
Memory	L1 D-Cache Size	KB	8	64	N/A	1024	16	32	32	64	32	32	16	16	64
	L1 D-Cache Associativity	Ways	1	2	N/A	4	4	8	128?	2	2	2	1	1	4
	L1 D-Cache Block Size	Bytes	32	64	N/A	64?	32	64	128	32	32	32	32	N/A	32
	L1 D-Cache Replacement Policy	N/A	N/A	X?	N/A	N/A	LRU	N/A	pseudo-LRU	LRU	LRU	N/A	N/A	N/A	pseudo-Random
	L1 D-Cache Latency	Cycles	2	3-4	N/A	2	Int: 1/2, FP: 3?	1/2?	1	Int: 1/2, FP: 3?	1?	2/3?	1?	2/3?	2
	L2 Cache Size	KB	96	<16384	1.75M	1024	256-4096	1024-131072	4096/8192	512-16384	512-4096	512-16384	1024-8192		
	L2 Cache Associativity	Ways	3	1	7	1	1	1,8	1,8	2	1?	1	1		
	L2 Cache Block Size	Bytes	64	64	X?	X?	32	128	128	64-128	64	64	64-512		
	L2 Cache Replacement Policy	N/A	N/A	X?	N/A	N/A	N/A	N/A	N/A	LRU	N/A?	N/A	N/A		
	L2 Cache Latency	Cycles	8	13	2	2	16-25	6-7	8-10	3/6/7?	7/9	12/14?			
Memory Latency First	Cycles	76?	X?	X?	X?	X	35	61?	X?	33/45/60/72?	60				
Memory Latency Following	Cycles	X?	X?	X?	X?	X	1?	X?	X?	33/7?	X?				
Memory Bandwidth	Bytes	16	8	8	8	8	8/16	16	8	16	16	32			
I-TLB Size	Entries	48	128	Micro I-TLB:4, Main: 96	160	128	128	256	Micro I-TLB: 8, Main: 64	Micro I-TLB: 1, Main: 64	64	L1: 16, L2: 128			
I-TLB Page Size	KB	1,8,64,512	1,8,64,512	4-16384	4-16384	128-8192	128-262144	4	4-16384	8,16,512,4096	4,64,512,4096	8,64,512,4096			
I-TLB Associativity	Ways	Full	Full	Full?	Full?	2	2	2	Full	Full	Full	L1: Full, L2: 2			
I-TLB Latency	Cycles	X?	13?	67	67	39-55	25-100s	70	32?	32?	32	X?			
D-TLB Size	Entries	64	128	128	128	128	128	128	8,16,512,4096	4,64,512,4096	8,64,512,4096				
D-TLB Page Size	KB	1,8,64,512	1,8,64,512	Full	Full	39-55	32?	32?	32?	32?	32?				
D-TLB Associativity	Ways	Full	Full	Full	Full	Full	Full	Full	Full	Full	Full				
D-TLB Latency	Cycles	X?	7?	4	4	4	4	4	4	4	4				
Misc	Decode/Issue/Commit Width	N/A	4	Decode: 4, Issue: 6	4	4	4	4	4	4	4	4	4	4	
	Pipeline Stages	N/A	7	7	7	7	6	5	5	5	5	9	9?	14	