

Joshua J. Yi

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OBJECTIVE

A full-time position on a cutting-edge research, design, or development design team.

EDUCATION

Ph.D., Electrical Engineering, University of Minnesota, 2003
M.S., Electrical Engineering, University of Minnesota, 1999
B.S., Electrical Engineering, University of Minnesota, 1996

RESEARCH INTERESTS

Simulation Methodology, Superscalar and Embedded Processor Design, Performance Analysis, Low Power Design, Benchmarking and Workload Characterization, Design Methodology and Optimization

PUBLICATIONS

Available at <http://www.arctic.umn.edu/~jjyi>

- J. Yi and D. Lilja, "Instruction Precomputation", *Speculative Execution in Modern Computer Architectures*, edited by P. Yew and D. Kaeli, To be Published.
- J. Yi and D. Lilja, "Computer Architecture", *Handbook of Innovative Computing*, edited by A. Zomaya, Springer-Verlag, To be Published.
- J. Yi, D. Lilja, and D. Hawkins, "A Statistically Rigorous Approach for Improving Simulation Methodology", *International Conference on High-Performance Computer Architecture*, February 2003
- J. Yi and D. Lilja, "Improving Processor Performance by Simplifying and Bypassing Trivial Computations", *International Conference on Computer Design*, September 2002
- J. Yi, R. Sendag, and D. Lilja, "Increasing Instruction-Level Parallelism with Instruction Precomputation", *Euro-Par*, August 2002
- J. Yi and D. Lilja, "An Analysis of the Amount of Global Level Redundant Computation in the SPEC 95 and SPEC 2000 Benchmarks", *Workshop on Workload Characterization*, December 2001

PROFESSIONAL ACTIVITIES

- **Co-Organizer** and **Co-Moderator** of the Panel: "The Future of Simulation: A Field of Dreams?", *International Symposium on Performance Analysis of Systems and Software*, March 2004.

WORK EXPERIENCE

Retek Inc., Minneapolis, MN

Engineering Intern

July 2003 – Present

- Determined the set of user-configurable parameters that had the largest effect on the execution time of the Retek Predictive Application Server (RPAS) retail software program.

Department of Electrical and Computer Engineering, University of Minnesota, Minneapolis, MN

Research Assistant

June 1999 – January 2003

- Showed that redundant computations are 24.4% of all instructions in typical programs. Created a technique to remove those computations to improve processor performance by 11.0%.
- Showed that trivial computations are 12.9% of all instructions in typical programs. Created a technique to bypass and remove those computations to improve processor performance by 8.2%.
- Developed processor scaling parameters to improve the accuracy of simulation results.
- Pioneered a novel statistically-based simulation methodology to improve the simulation process.
- Developed a novel method of benchmark and input set characterization to reduce the total simulation time.
- Characterized the spatial behavior of load instructions in the SPEC 2000 benchmark suite.
- Directed the Verilog behavioral design of the Superthreaded Architecture.
- Determined potential operating ranges for nanotechnology tunneling-phase logic devices.

Teaching Assistant

March 1997 – May 2003

- Taught EE 5940, Introduction to Computer Architecture (Gave lectures, wrote and graded tests, and assigned grades)
- Created grading guidelines to improve the consistency of the laboratory grading process.
- Evaluated and graded potential and actual designs for a frequency specific AM radio; a Frequency Synthesizer using a Phase-Lock Loop; and an Active Infrared Motion Detector.

Summit Design Inc., New Brighton, MN

Engineering Intern

June 1998 - September 1998

- Created Verilog and VHDL verification programs for the virtual CPU ARM940T solution.

Fisher-Rosemount Inc., Eden Prairie and Chanhassen, MN

Engineering Co-op

June 1994 - September 1997

- Wrote the test specification to verify the implementation of the Pressure Transmitter Enhancement Software.
- Implemented a manufacturing time tracking package to improve the efficiency of the manufacturing process.
- Designed tests to verify the functional correctness of a next-generation ASIC.
- Determined the effects of temperature and electrostatic discharge on thin-film and wire-wound resistance-based temperature sensors to improve their manufacturing yield.

SKILLS

C, Verilog, VHDL, SimpleScalar, csh/tcsh, Quickturn Speedsim, Spice, Word, Excel, Powerpoint

RELEVANT COURSES

Computer Architecture, Parallel Computer Organization, Computer-Aided Design, CAD for VLSI Interconnects, VLSI Design, Applied Switching Theory, Design of Digital Circuits, Analog I.C. Design, Digital Signal Processing and Laboratory, Statistics

HONORS

Dean's List, Outstanding TA of the Year

WORK STATUS

U.S. Citizen